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EXAMINER	
STARK, JARRETT J	
ART UNIT	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/797,463	YEO ET AL.	
	Examiner	Art Unit	
	Jarrett J. Stark	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *3/14/2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *12-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *12-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments filed 3/14/2008 have been fully considered but they are not persuasive.

Applicants submit that the prior art reference Maegawa dos not disclose or suggest "wherein the source and drain regions are vertically formed to cover the sides of the active region in other patterns adjacent to sides of the spaced apart patterns; and forming a vertical source electrode electrically connected to the source region and a vertical drain electrode electrically connected to the drain region." nor "forming a horizontal channel including at least two horizontal channel regions formed in spaced apart patterns; and forming source and drain regions in other patterns at sides of the spaced apart patterns."

In response, as presented in the previous Office Action, source and drains are inherent features, which are located on opposite sides of and in direct contact with the corresponding channel. In the case of the prior art, Maegawa clearly depicts a transistor having multiple vertically stacked channels, where each channel is inherently required to have a source and drain. Each inherently required source and drain will be inherently located on opposite sides of and in direct contact with the corresponding vertically stacked channel. Since the channels are shown to be vertically stacked it naturally follows that the required sources and drains will too be vertically stacked. (See Maegawa - Embodiment 16, provided below.)

In the cited Embodiment Maegawa disclosed the stacked channel structure is form by merely repeating the previous disclosed process steps to for the layered structure. Specifically, "transistor having five layers of channel silicon film 3" (3a, 3b, 3c, 3d, and 3e). Maegawa disclosed in the previous embodiments that the source/drains are formed in the channel silicon film after patterning takes place. Thus, even though Maegawa is silent on the fact that the sources and drains are vertically stacked it is clearly apparent that they are vertically stacked.

> *(153) (Embodiment 16)*
>
> *(154) The transistor in Embodiment 15 has a channel silicon film formed of two layers 3a and 3b. However, further multiple layers of channel silicon film, e.g., three, four or more layers may be formed.*
>
> *(155) FIG. 30 shows a cross-sectional view of a transistor having five layers of channel silicon film 3. As shown in FIG. 30, first silicon oxide film 2 is formed on silicon substrate 1, and first and second gate silicon films 22 and 23 and third to fourth gate silicon films 25 to 27 are successively laid one on top of another over first silicon oxide film 2. A channel silicon film 3a is formed between first gate silicon film 22 and second gate silicon film 23; a channel silicon film 3b, between second gate silicon film 23 and third gate silicon film 25; a channel silicon film 3c, between third gate silicon film 25 and fourth gate silicon film 26; and a channel silicon film 3d, between fourth gate silicon film 26 and fifth gate silicon film 27. Further, a channel silicon film 3e is formed on fifth gate silicon film 27.*
>
> *(156) In the transistor shown in FIG. 30, channel surfaces are formed on the opposite sides of channel silicon film 3a by first gate silicon film 22 and second gate silicon film 23. Similarly, channel surfaces are formed on the opposite sides of each of channel silicon films 3b to 3d. One channel surface is formed on the lower side of the channel silicon film 3e. Accordingly, the transistor shown in FIG. 30 has nine channel surfaces and therefore has a markedly improved current drive capacity.*
>
> *(157) The method of manufacturing the transistor shown in FIG. 30 will be described. The process steps of Embodiment 15 are repeated a certain number of times to laminate multiple layers of gate silicon and silicon*

> *nitride films. Thereafter, the operation of patterning and the operation of removing silicon nitride film are repeated from the uppermost gate silicon film to obtain a structure in which multiple layers of bridge-like gate silicon film are laid one on top of another. Thereafter, gate insulating films and channel silicon are successively deposited as in the case of Embodiment 15. In this manner, a transistor in which five channel silicon films are superposed as shown in FIG. 30 can be formed.*
>
> *(158) Other structures in which a larger number of channel silicon films are superposed can be obtained in the same manner.*

Regarding the further arguments that Maegawa does not disclose or suggest the claimed limitations of claim 23, because "the Office Action arbitrarily combines the embodiments of Maegawa to teach the recitations of claim 23." With this statement it is acknowledged by the Office that the Applicants agree Maegawa does disclose the recited claim limitations.

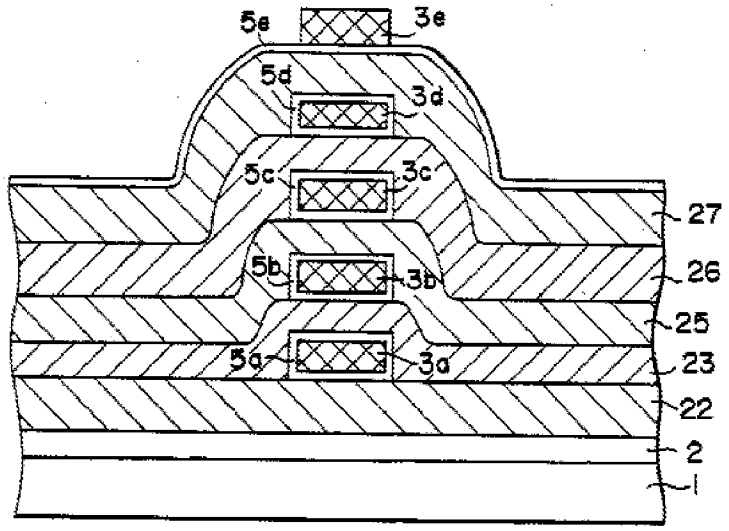
Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 12- 19 and 30 are rejected under 35 U.S.C. 102(b) as being anticipated by Maegawa (US 5,583,362).

FIG. 30

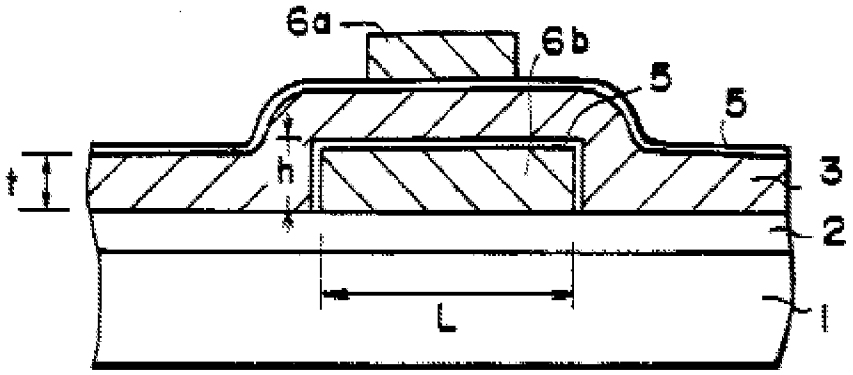


Regarding claims 12 and 30, Maegawa discloses a method of forming a unit cell of a metal oxide semiconductor (MOS) transistor, comprising:

forming a MOS transistor on an integrated circuit substrate including an isolation layer (fig. 30 layer 2) and an active region higher than the isolation layer (Fig. 30, layers 3a, 3b, 3c, 3d, 3e,...), the MOS transistor having a source region and a drain region (not shown due the cross-sectional view of figure 30, however source and drains are inherently required to be adjacent either side of each channel. A channel can not function without a source and drain) on the isolation layer, and a plurality of gates on the active region, the plurality of gates being stacked (Fig. 30, layers 22, 23, 25, 26, 27,...) between the source region ant the drain region (not shown due the cross-sectional view of figure 30, however source and drains are inherently required to be adjacent either side of each channel. A channel can not function without a source and drain);

forming a horizontal channel between the source and drain regions, the horizontal channel including at least two horizontal channel regions formed in spaced apart patterns (Fig. 30), wherein the source and drain regions are vertically formed to cover the sides of the active region in other patterns adjacent to sides of the spaced apart patterns (not shown due the cross-sectional view of figure 30, however source and drains are inherently required to be adjacent either side of each channel. A channel can not function without a source and drain)

FIG. 15



Regarding claim 13, Maegawa discloses the method of claim 12, wherein forming the at least two spaced apart horizontal channel region comprises: forming an active region on the integrated circuit substrate; and forming at least one epitaxial pattern on the active region and spaced apart from the active region (Col. 5 lines 5-20).

Regarding claims 14 & 15, Maegawa discloses the method of claim 13, wherein forming the at least one epitaxial pattern comprises forming first and second epitaxial

patterns, the second epitaxial pattern being on the first epitaxial pattern and spaced apart from the first epitaxial pattern, the method further comprising: forming a mask pattern on the second epitaxial pattern (Col. 5 lines 5-20 & Col. 1 line 65 → Col. 2 line 9 - patterned by photolithography will inherently involve masks).

Regarding claim 16, Maegawa discloses the method of claim 12, wherein forming the source and drain regions comprises forming vertical source and drain regions, the vertical source region being on a first side of the horizontal channel region and the vertical drain region being on a second side of the horizontal channel region and spaced apart from the vertical source region (Fig 15 & Col. 6 lines 53-57).

Regarding claim 17, Maegawa discloses the method of claim 16, further comprising: forming a gate pattern (Fig 30-[26]) on the horizontal channel (Fig 30-[3c]) and between the at least two spaced apart horizontal channel regions (Fig 30-[3c and 3d]); and forming a gate insulation layer (Fig 30-[5c and 5d])between the gate pattern and the at least two spaced apart horizontal channel regions.

Regarding claim 18, Maegawa discloses the method of claim 17, further comprising:

forming a first insulation pattern (Fig 15. – insulation layers [2] and/or [5]) between the source and drain electrodes and the integrated circuit substrate and between the gate pattern and the integrated circuit substrate.

Regarding claim 19, Maegawa discloses the method of claim 18, further comprising: forming a mask pattern on the horizontal channel, wherein the gate pattern extends between an upper channel region of the at least two spaced apart horizontal channel regions and the mask pattern (Col. 5 lines 5-20 & Col. 1 line 65 → Col. 2 line 9 - patterned by photolithography will inherently involve masks).3

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

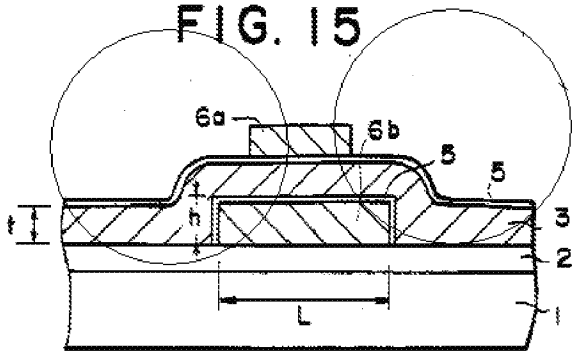
> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 20 –29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Maegawa (US 5,583,362) as applied in claim 19 above and in further view of Nakajima (US 6,420,758).

Regarding claim 20, Maegawa in view of Nakajima discloses the method of claim 19, further comprising: forming a second insulation pattern (Fig. 15 – [5]) on the horizontal channel and the vertical source and drain regions (Fig. 15 – [3] – source and

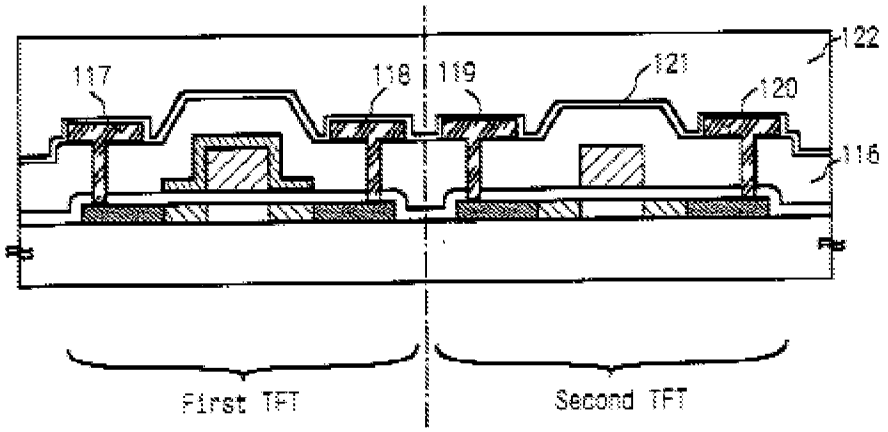
drain regions left and right of gate 6a), wherein the second insulation pattern defines a gate opening on the horizontal channel (Fig. 15 – circled by Examiner for clarity), wherein the gate pattern is provided in the gate opening and

FIG. 15



Maegawa does not explicitly disclose wherein the source and drain electrodes extend through the second insulation pattern and are connected to the vertical source drain regions. It is however notoriously well known extend the source and drain electrodes through the insulation pattern to make electrical contact with the source and drain electrodes. An example of this is shown by Nakajima in Figure 2E below. The figure shows a commonly used method of connecting source and drain electrodes to the source and drain trough an insulating layer.

FIG. 2E



It would have been within the scope of one of ordinary skill in the art at the time of the invention to combine the teachings of Maegawa and Nakajima to enable the source/drain electrode formation step of Maegawa to be performed according to the teachings of Nakajima because one of ordinary skill in art at the time of the invention would have been motivated to look to alternative suitable methods of performing the disclosed source/drain electrode formation step of Maegawa and art recognized suitability for an intended purpose has been recognized to be motivation to combine. MPEP 2144.07.

Regarding claim 21, Maegawa in view of Nakajima discloses the method of claim 20, further comprising: forming a third insulation pattern on the second insulation pattern and the gate pattern, wherein the source and drain electrodes extended through the third insulation pattern (Nakajima, layer [116]) and the second insulation pattern and are connected to the vertical source and drain regions.

Regarding claim 22, Maegawa in view of Nakajima discloses the method of claim 21, wherein an upper surface of the first insulation pattern is higher relative to a lower surface of the gate pattern. (Maegawa, Fig. 15 first insulating layer [5] is above lower gate pattern [6b])

Regarding claim 23, Maegawa in view of Nakajima discloses a method of fabricating a transistor comprising:

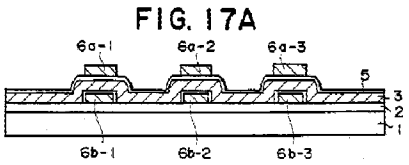
forming a trench region on an integrated circuit substrate to define an active region (Maegawa, Fig. 1A);

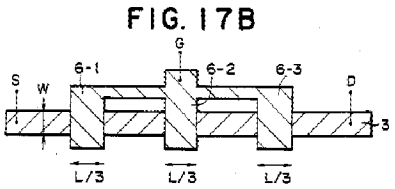
forming a stacked structure including at least one set of first epitaxial patterns and second epitaxial patterns on the active region (Maegawa, Fig. 30);

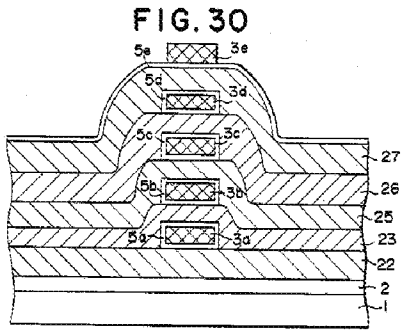
forming a first insulation pattern on a floor of the trench (Maegawa, Fig. 1B);;

growing a third epitaxial layer on sidewalls of at least one set of first and second epitaxial patterns(Maegawa, Fig. 1A);

forming a second insulation pattern on a surface of the integrated circuit substrate, the second insulation pattern defining a gate opening that exposes at least a portion of the third epitaxial layer (Figs 17A-B & 30);







;

removing the third epitaxial layer in the gate opening to expose the set of at least one first and second epitaxial patterns (Maegawa, Figs 17A-B & 30);

selectively etching the first epitaxial patterns of the set of at least one first and second epitaxial patterns to form a horizontal channel region having a plurality of spaced apart channel layers (Maegawa, Col. 5 lines 5-20 & Col. 1 line 65 → Col. 2 line 9);

forming a gate oxide layer on a surface of channel layers (Maegawa, layer [5]);

forming a gate pattern on the horizontal channel and in gap regions between the channel layers and the gate opening (Maegawa, Figs 17A-B & 30); and

forming source and drain electrodes penetrating the second insulation pattern to be connected to the third epitaxial layer (Nakajima, Figure 2E).

Regarding claim 24, Maegawa in view of Nakajima discloses the method of claim 23, wherein forming the trench and a stacked structure further comprises: alternately stacking sets of first and second epitaxial layers on the integrated circuit substrate; and patterning the sets of the first and second epitaxial layers and the integrated circuit substrate to form a trench, and sets of the first and second epitaxial patterns (Maegawa, Col. 5 lines 5-20 & Col. 1 line 65 → Col. 2 line 9 & Figs 17A-B & 30).

Regarding claim 25, Maegawa in view of Nakajima discloses the method of claim 23, wherein the first and third epitaxial layers comprise silicon and wherein the second epitaxial layer comprises silicon germanium.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to form the second epitaxial layer of silicon germanium, since it has been held to be within the general skill of a worker in the art to select a known material on the base of its suitability, for its intended use involves only ordinary skill in the art. *In re Leshin*, 125 USPQ 416.

Regarding claim 26, Maegawa in view of Nakajima discloses the method of claim 23, wherein an upper surface of the first insulation pattern is formed lower relative to the first epitaxial layer (Maegawa, Fig. 15 first insulating layer [5] is above lower gate pattern [6b]).

Regarding claim 27, Maegawa in view of Nakajima discloses the method of claim 23, wherein forming the second insulation pattern is preceded by: forming an etch stop layer conformally on a resultant structure including the third epitaxial layer (Maegawa, Figs 30 shows that the top epitaxial layer is patterned with out affecting the insulating layer directly below it, therefore obviously indicating that the insulating layer is an etch stop), wherein forming the gate opening comprises sequentially patterning the second insulation pattern and the etch stop layer and wherein the source and drain electrodes penetrate the etch stop layer (Nakajima, Figure 2E) to be connected to the third epitaxial layer (Maegawa, Col. 5 lines 5-20 & Col. 1 line 65 → Col. 2 line 9).

Regarding claim 28, Maegawa in view of Nakajima discloses the method of claim 23, wherein forming the second insulation pattern is preceded by: implanting impurities in the first and second epitaxial layers to form channel doped layers; and implanting impurities into the third epitaxial layer to form source and drain regions (Maegawa, Fig 15 & Col. 6 lines 53-57).

Regarding claim 29, Maegawa in view of Nakajima discloses the method of claim 23, wherein forming the stacking structure of the first and second epitaxial patterns further comprises forming a mask pattern at the upper most layer, and wherein the first and second epitaxial patterns are alternately stacked (Maegawa, Col. 5 lines 5-20 & Col. 1 line 65 → Col. 2 line 9 – photolithography is used to pattern the repeated layers shown in Figs 17A-B & 30, there for is obvious that the upper most layer will have a mask to form the pattern).

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jarrett J. Stark whose telephone number is (571) 272-

6005. The examiner can normally be reached on Monday - Thursday 7:00AM - 5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Jarrett J Stark
Examiner
Art Unit 2823

JJS
May 12, 2008

/Michelle Estrada/
Primary Examiner, Art Unit 2823